A Novel Multi-Bit Parallel ΔΣ FM-to-Digital Converter with 24-bit Resolution

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Abstract

This paper describes a multi-bit ΔΣ FM-to-digital converter (FDC) combining 1024 first-order ΔΣ modulators in parallel to increase the signal to quantization-noise ratio (SQNR). This parallelization technique is totally new and according to theory, the SQNR is increased by 6 dB per doubling of number of modulators. The proposed circuit is an extension of the existing frequency delta sigma modulator (FDSM)-concept. The FDSM-concept is based on a ΔΣ-modulator with no global feedback and thus no need for a feedback DAC, which makes multi-bit conversion straightforward. Theoretical discussions and circuit simulation are presented along with measured results from a 24-bit parallel FDC which has been implemented in a standard 0.6μm CMOS process from Austria Micro Systems AG (AMS). For a 150 Hz bandwidth the measured SQNR is 146 dB with a clock frequency of 20 MHz.

1. Introduction

The resolution of a conventional ΔΣ-modulator is determined mainly by the oversampling-ratio and modulator order. However, when trying to increase either of them different challenges arise. Due to parasitic analog components, the bandwidth of the circuit elements in the modulator is limited. The benefit of increasing the sampling clock frequency will therefore only be useful to a given extent. Increasing modulator order is in theory a more efficient way to extend the dynamic range, but when dealing with practical circuits having non-ideal components, modulator instability and component matching become severe problems especially for higher order circuits. Recently a new class of modulators with multi-bit output have been object for research. This kind of modulator, usually called a multi-bit ΔΣ modulator can give high SQNR for a modest oversampling ratio and low modulator order. However, for the conventional ΔΣ modulator with a global feedback, the linearity of the multi-bit feedback DAC is very critical [4]. Different methods for improving linearity of the feedback DAC are reported in the literature, but the introduction of correction techniques gives more complexity in the design process [1, 2, 3]. The new topology proposed in this paper is based on the FDSM-concept [5, 6] which has no global feedback. The lack of linearity in the multi-bit feedback DAC is therefore not even a topic with the proposed converter. A first order FDSM-modulator is illustrated in Fig. 1. The circuit is simply two D flip-flops and a XOR-gate performing modulo differentiation. The input signal is a FM-signal while the output signal is a conventional ΔΣ bit-stream. The extremely small size of this modulator makes it possible to integrate a large number of them on a single chip. The basic idea behind the work in this paper is to take advantage of the fact that the quantization-noise from two delta sigma bit-streams are uncorrelated when the input signals are delayed versions of the same FM-signal, while the modulating signal itself is heavily correlated. Then by summing the outputs of a high number of FDSM-modulators operating on delayed versions of the same signal, the SQNR will be increased. The theory behind the proposed converter is discussed in section 2 while the measured results from the actual circuit implementation is presented in section 3. Finally the conclusion is presented in section 4.

2. Open ended delay-line FDSM parallelization

In a FDSM-converter as illustrated in Fig. 1, the frequency of the modulating input signal will be very small compared to both the FM-carrier and the sampling clock. By feeding the FM-signal into an analog delay-line with k tappings connected to separate FDSM-modulators, the result will be k different ΔΣ bit-streams where the different baseband signals are almost 100 percent correlated. The ideal situation will be when the total delay through the analog delay line is equal to one half period of the FM-
carrier, but the delay can also be larger as will be shown later in this section. By adding these outputs together the SQNR will increase if and only if the in-band quantization noise is uncorrelated. The total system as illustrated in Fig. 2 will be a parallelized feed-forward multi-bit \( \Delta \Sigma \) modulator.

![Diagram](image)

**Figure 2.** \( k \) parallel FDSM converters operating on delayed versions of the same FM-signal.

In many cases the quantization noise of a \( \Delta \Sigma \) modulator can be considered to be white. The correlation between the quantization noise from two different FDSM-modulators operating on delayed versions of the same FM signal will thus be very small. The result of adding the quantization noise from a large number of FDSM-modulators together will therefore not increase the total noise power significantly. The ideal situation as described above requires that the delay is equally distributed along the analog delay-line and that the total delay equals one half period of the FM-carrier. However, in a practical application one will have to take into account the effect of different non-idealities like non-uniform delay distribution and the case when the total delay differs from one half period of the FM-carrier. To analyze the impact these non-idealities will have on the total quantization-noise we will start with the definition of the total phase-error integrated over all the bit-streams for a given time-sample:

\[
\varepsilon_{\text{total}}^n = \sum_{i=0}^{k-1} \varepsilon_{ln}^i = \sum_{i=0}^{k-1} \text{mod}_{\pi}(\Theta_n - \Phi_l)
\]

where \( \varepsilon_{ln}^i \) is the phase quantization error of bit-stream number \( l \) at time sample number \( n \). \( \Theta_n \) is the position of a falling or raising edge of the FM-signal at the input of the delay line, while \( \Phi_l \) is the actual delay of tapping number \( l \). In Fig. 3 the quantization errors for a three tapping delay line FDSM with a total delay of less than \( \pi \) are shown. By studying the figure it is obvious that the sum of the three errors will be a periodic function according to Eq. 1 with a period of \( \pi \). The amplitude of the quantization error is determined by the total phase delay along the line relative to \( \pi \). As an example we can look at the situation where we have three delay elements with four different tappings. In Fig. 4, the total quantization error is plotted versus sampling edge position for different total delays up to \( \pi \), and as we can see that the amplitude start with a value of 4 for the case of no delay, and is reduced to 1 for the case when the delay is equal to \( \pi \). The case of no delay will be equal to a single FDSM-converter, since both the signal amplitude and the quantization noise is increased by a factor of four, giving a net improvement of 0. The optimum case will be when the total delay is \( \pi \) increasing the SQNR by a factor of four compared to a single FDSM. The total error when the delay is more than \( \pi \) may be calculated in the same way as illustrated in Fig. 5. The amplitude of the different curves will then be less different with a larger minimum amplitude and a smaller maximum amplitude, making it less sensitive to variations in the total phase delay. The above results tells us that in the case of a non-modulated FM-signal, the quantization noise will have a theoretically minimum when the total delay is \( \pi \). However as the FM-signal becomes heavily modulated, the situation will be changed, and the average noise might be reduced by choosing a total line delay of a higher integer multipium of \( \pi \). To see how the total quantization noise will vary versus total phase-shift along the delay-line, a 90-tapping FDSM was simulated using Matlab. For the ideal case with equally distributed phase delays, the result
Figure 5. Total quantization error for different line-delays relative to the FM-signal. Stipples: $2\pi$ delay to the last tapping. Dots: $2.4\pi$ delay to the last tapping. Solid: $3\pi$ delay to the last tapping.

is plotted in Fig. 6. The result is a curve following a sinc-shape having a global minimum at $\pi$, and local minimums around higher multiples of $\pi$. However, there are some spikes at the exact points where the delays are $n$ times $\pi$. These spikes are caused by the increased correlation between different quantization-noise samples. If we add 10 percent mismatch to the delay elements, as typically will be the case for a practical implementation, the correlation will be reduced and the spikes becomes less significant as illustrated in Fig. 7. However, the average noise level is increased.

3. A 24-bit 1024 parallel FDSM

To verify the theory in the previous section, a circuit prototype was designed and fabricated in a standard double-poly 0.6um process from AMS. The prototype has an analog delay-line with 1024 tappings, each connected to a separate first-order D flip-flop FDSM. The output of all the modulators are added together using a pipelined adder-tree structure having an 11-bit output. The 11-bit delta-sigma word stream is then fed into a second-order sinc-type decimation filter. The layout of the circuit with explaining markers is illustrated in Fig. 8. To determine

the theoretical resolution of this converter, we start with defining the resolution of a single D flip-flop FDSM:

$$\text{SQNR} = 20 \log \left( \frac{3}{2\pi} \right) + 20 \log \left( \frac{\Delta f}{f_{bw}} \right) + 10 \log(f_{clk})$$

In this equation $\Delta f$ is the maximum deviation of the FM-signal, $f_{bw}$ is the bandwidth of the modulating signal while $f_{clk}$ is the sampling clock frequency. According to theory, the resolution may be increased by $20 \log(1024)dB = 60dB$ for the ideal case when the total line-delay is $\pi$ and the FM-signal is unmodulated. However as explained in the previous section, the increased
resolution will be smaller for a practical circuit with a heavily modulated input signal where the delaying elements are subject to mismatch.

3.1. Measured results

From Fig. 5 we can see that the expected resolution improvement will be about 50 percent of the theoretical value when choosing a line delay of $2\pi$ or $4\pi$ and 10 percent deviation of the FM-signal. As a rough estimation we can then expect to increase resolution with about 30 dB compared to a single DFF-FDSM. A number of measurements were performed to verify the expectations. First we had to determine the actual delay of the analog delay-line which were measured to be 150 ns. This means that we will have to use a carrier frequency that must be a multiple of 3.30 MHz ($\pi$). For the first measurement we have a FM-signal with a carrier frequency of 6.6 MHz and a deviation of 1.1 MHz. The delay line now holds one period of the FM-signal. The sampling clock frequency is 20 MHz. The power spectral density (PSD) of the measured output signal is plotted in Fig. 9 and the SQNR is calculated to 146 dB for a signal bandwidth of 150 Hz, which is slightly below the expected value of 152 dB.

For the next measurement we have a carrier frequency of 6.6 MHz and a deviation of 1.5 MHz. One period of the FM-signal is still in the delay-line, and the clock frequency is 20 MHz. The PSD of the output-signal is plotted if Fig. 10. The resolution in a 20kHz bandwidth is measured to 85 dB, which is 6dB below the expected value of 91 dB. The harmonic components seen in both the figures are generated by the FM-signal source. We used an Agilent 33120A which has a specified harmonic distortion of -70 dBc, and the measured distortion is within this range. The chip has 176000 transistors and a physical size of 20mm². The power consumption was measured to 0.5 W for a supply voltage of 5 volt.

4. Conclusion

A novel 24-bit $\Delta\Sigma$ frequency-to-digital converter combining 1024 single $\Delta\Sigma$ FDSM-converters in parallel has been designed and fabricated in a standard 0.6 um CMOS-process. The measured results shows an improved SQNR of about 20 dB compared to the case of a single D flip-flop FDSM-converter. The topology is insensitive to both component mismatch and phase-noise at the FM-signal input, making the circuit design straightforward. The measured SQNR is 146 dB in a bandwidth of 150 Hz. The power consumption is 0.5 W @ 5V.


