RF MEMS – new possibilities for future wireless systems

by

Oddvar Søråsen

NANO - nanoelectronics group
Department of Informatics
University of Oslo
Overview of presentation

- Department of Informatics and the NANO group
  - MEMS as an extended activity of the NANO group
- What is RF MEMS?
  - Challenges by implementing a "radio-on-a-chip"
    - Example:
      - Filter based on resonating mechanical structures
- From MEMS devices to "smart integrated systems"
  - How to integrate CMOS and MEMS?
    - Examples:
      - CMOS – MEMS monolithic oscillator
      - CMOS – MEMS inductors
- Future plans
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University of Oslo

Faculty of Theology
Faculty of Arts
Faculty of Law
Faculty of Dentistry
Faculty of Medicine
Faculty of Social Sciences
Faculty of Education

Faculty of Mathematics and Natural Science

Institute of Theoretical Astrophysics
Department of Biochemistry
Department of Chemistry
Department of Physics
Department of Geophysics
Department of Biology
School of Pharmacy
Department of Mathematics
Department of Geography

Department of Informatics

UoO: 30 000 students, 4600 employees
**Ifi - main research directions**

- **Software Technology**
  - Object orientation: SIMULA
- **Distributed Systems**
- **Information Systems**
- **Microelectronic Systems**
- **Computational Science**
  - Splines

Splines for geometry and radiance rendering

Professors O.J. Dahl and Kristen Nygaard: von Neumann medal, Turing award, Commanders of St. Olaf Order
Who are we?

- “Nanoelectronics” (NANO) is a research group within the strategic area of “Microelectronic Systems”

- NANO has recently been selected as ”Utviklingsmiljø” by MNFak (5 years)
  - Vision: ”The Nanoelectronics research group is to be recognized as an international top group within the field low-power nano-/microelectronics for wireless sensor networks”

- Prizes for quality in education and teaching environment
  - ”Kunnskapsdepartementets utdanningskvalitets pris 2006”
  - ”Universitetets læringsmiljøpris 2005”
Members of the NANO group

- **Faculties**
  - Dag T. Wisland (group leader)
  - Yngvar Berg
  - Tor Sverre Lande
  - Oddvar Søråsen

- **Part time faculties/researchers**
  - Philipp Häfliger (100%)
  - Snorre Aunet (100%)
  - Tor Fjeldly (UNIK) (20%)
  - Alf Olsen (Micron) (20%)
  - Joar M. Østby (SINTEF) (20%)

- **Ph.D students**
  - Jens Petter Abrahamsen
  - Henning Gundersen
  - Håkon A. Hjortland
  - Rene Jensen
  - Johannes Lomsdalen
  - Jørgen Michaelsen
  - Omid Mirmotahari
  - 3 in process

- **Engineers**
  - Håvard Kolle Riis
  - Hans K. O. Berge (33%)
Research focus

- Developing systems based on **integrated electronics (VLSI)**
  - full-custom design of analog, digital and mixed-mode circuits
  - prototyping and verification
- Emphasizing **low power** circuits
- Future **miniaturization** demands deep insight into the technology
  - modeling non-ideal effects
Research activities (1)

- **Data conversion and sensor interfacing**
  - new principles for implementing Delta-Sigma ADC, DAC

- **Micro power digital signal processing**
  - new circuit principles – subthreshold operation
  - compact ultra low power CMOS – redundancy – defect tolerance
    - patent appl “Birkeland Innovasjon”

- **Bio-inspired microelectronics**
  - nevromorph engineering
  - neural inspired micro-architectures
  - new ways of coding signals for transmission
Research activities (2)

- Low power radio communication
  - Ultra Wideband Impulse Radio
  - Short range radar for medical applications
    - Novelda AS
- Combination of CMOS and micro/nano-mechanics (MEMS/NEMS)
  - Nanoelectronics and sensors
  - RF front-end
  - Integration: CMOS - MEMS

- The research contains central ingredients in implementing future smart, integrated, wireless sensor nodes
  - Goal: develop a low power node in a wireless sensor network (WSN)
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MEMS in electronic systems

- **National initiative** to establish micro and nano technology in Norway
  - Norwegian Research Counsel
  - **MiNaLab** in neighbouring building (SINTEF and UiO)
    - on sabattical leave 03/04
- MEMS a **new degree of freedom** to implement integrated systems
  - microelectronics can **use** micromechanical components
  - MEMS structures would **need** an electronic framework
- Suitable **competence** at MES
  - modeling, analysis, implementation of VLSI from transistors to complex systems
Selecting a focus → RF MEMS

- "RF MEMS refers to the design and fabrication of dedicated MEMS for RF (integrated) circuits"

- Challenging, promising and exciting field!
- Close connection to circuit technique

- An increasing number of applications of MEMS in RF
- Large market: wireless communication
  - telecommunication, mobile phones
  - distributed intelligence (observation, activation)
  - environmental surveillance

- Consistent with IFI/MES strategic activity → Wireless Sensor Nets
- A new course established, 2005: INF5490 RF MEMS
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Typical RF MES components

- Switches
- Variable capacitors
- Inductors
- Resonators
- Micromechanical filters
- Phase shifters
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→ focusing on real vibrating structures

- Can be used to implement
  - oscillators
  - filters
  - mixer with filter
Comb resonator

lateral movement
Beam resonator (clamped-clamped)

First-order resonant frequency:

\[ f_r = 1.03 \sqrt{\frac{E}{\rho}} \frac{t}{L^2} \]

- \( E \): Young’s modulus
- \( \rho \): Density
- \( t \): Beam thickness
- \( L \): Beam length

vertical movement
Appealing advantages given by RF MEMS

- Higher **performance**
  - increased selectivity
  - higher Q-factor
  - reduced loss
  - better isolation
  - low distortion
  - increased bandwidth
- Lower **power dissipation**
- Lower **cost**
  - batch processing
- Circuit and system **miniaturization**
  - monolithic integration with IC or by packaging!
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Challenges by implementing transceivers

- **Performance**
  - todays RF systems need **off-chip components** to obtain required performance
    - matching networks, filters, oscillators etc.

- **Miniaturization**
  - discrete components are a hinder

- **Reconfiguration**
  - increased requirements to cover a variety of standards and channels
  - **reconfigurable front-end** for ”sw-defined radio” is needed

- RF MEMS components can be used as
  - A) **Replacement** for discrete passive components
  - B) **New** integrated **functionality**
    - new system architectures
Miniaturization of Transceivers

- Need high-\( Q \) \( \Rightarrow \) small BW with low loss

- High-\( Q \) functionality required by oscillators and filters cannot be realized using standard IC components \( \Rightarrow \) use off-chip mechanical components

- SAW, ceramic, and crystal resonators pose bottlenecks against ultimate miniaturization

C. T.-C. Nguyen
Univ. of Michigan
A large number of off-chip high-Q components replaceable with \( \mu \)machined versions; e.g., using \( \mu \)machined resonators, switches, capacitors, and inductors.

C. T.-C. Nguyen

Univ. of Michigan
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Master project (finished)

- Micromechanical filter by resonating beams
  - H structures
- Master student Ole-Petter Arhaug
- Modeling
  - analytical, FEM
- Simulations with CoventorWare, Cadence
- Design according to a specific process: QinetiQ
  - QinetiQ INTEGRAM processes, a part of Europractice

State-of-the-art tool for FEM analysis: **CoventorWare**

- “Bottom-up” procedure:
  - 1) Build a 3D model
    - build by “stacking layers” (structural and sacrificial layers)
    - deposit layers - etch patterns - release
  - 2) Partition the model (“meshing”)
    - tetrahedrons, Manhattan bricks
  - 3) Apply “solvers” on sub-elements
    - electrical/ mechanical/ coupled
    - iterate
Process specification

- Specify a **process file** which matches an actual foundry process
  - simplifications
  - realistic: essential process features included
Layout

O-P Arhaug
3-D model building

O-P Arhaug
Meshed 3D model for FEM analysis

O-P Arhaug
Filter operation: 2 identical resonators

In phase

Out of phase
CoventorWare simulations for 6 resonating modes (O-P Arhaug)
Harmonic response for given dampings

(a) 0.1

(b) 0.001

O-P Arhaug
Vision: Micromechanical signal processing

- Signal processing function implemented by interconnection of MEMS resonators
- Data is being processed in the frequency domain
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Combining MEMS and IC

- A strong demand exists for making combined MEMS – CMOS systems
- MEMS devices need surrounding µelectronics

Fig. 4: Circuit schematic for the µresonator oscillator.
μelectronic systems can be extended with MEMS devices for contacting the environment
How can µelectronics and MEMS be combined?

- **Multi-chip**
  - traditional method: SiP, SoP
  - separate, different processing lines involved
    - optimal processing of sub-modules
  - combination of quite diverse technologies
    - Si, glass, plastic, organic
  - heavy load impedances, parasitics
  - costly, work intensive
The ultimate goal

- SoC – System-on-Chip
  - easier handling
  - lower production costs
  - reduced parasitics
  - higher reliability
  - equal or higher performance!?

- \( \rightarrow \) Cheaper and more standardized procedures and processes are needed!
Typical features

- **MEMS features**
  - a diversity of different processing lines exist
    - special features and secrets
    - limited interoperability
  - designers with background in physics, material technology, chemistry
    - working close to MEMS labs

- **CMOS features**
  - standardized processes
  - design activity and semiconductor processing is separated
    - foundry concept, second sourcing
  - have expanded the design community

- **Future MEMS/CMOS designers**
  - Designers with background in computer science, ASIC design
  - Working on a conceptual level, separated from processing details
  - Handling geometries
Methods for on-chip integration

- **pre-CMOS**
  - MEMS before CMOS

- **intermediate-CMOS**
  - Mixed MEMS/CMOS

- **post-CMOS**
  - CMOS before MEMS
Methods for on-chip integration

- pre-CMOS
  - MEMS processing is done first
  - Coars-grained MEMS steps introduce topographic variations on the wafer surface
  - Planarization before CMOS processing
  - Reluctance to take "dirty" wafers into CMOS process lines
MEMS → CMOS

Sandia Embedded Process

1. Trench etched into Si using KOH
2. MEMS fabricated in trench
3. Trench filled with LPCVD oxide
4. Trench planarized with CMP
5. MEMS stress anneal
6. Trench seal with LPCVD nitride
7. Standard CMOS fabrication next to MEMS
8. CMOS passivated with PECVD nitride
9. Trench opened, MEMS released
Methods, cont.

- intermediate-CMOS
  - Certain steps in the CMOS process are modified
  - Intertwined process which hinders optimization of each “processing module” separately

*Figure 12.28.* Cross section of the sensor area in Analog Devices’ BiMOSII process [47].

BiMOSII combination process from Analog Devices used for implementing accelerometers
Methods, cont.

- **post-CMOS**
  - An ordinary CMOS process is used first
  - MEMS processing steps are added

  - **High temperature** can destroy the CMOS metallization
    - Use special CMOS metal layers (e.g. tungsten) to withstand high temperature
    - Use **lower temperature** when depositing structural MEMS materials
      - Specific structural materials can be used, SiGe

  - Generally, a **whole wafer** must be post-processed
    - Different dimensions in MEMS and CMOS processing lines
    - Post processing single chips is not practical if masking is needed
Surface Micromachining

- Release Etch Barrier
- Structural Material (e.g., polysilicon, nickel, etc.)
- Sacrificial Oxide
- Hydrofluoric Acid Release Solution
- Free-Standing Resonator Beam

Fabrication steps compatible with planar IC processing

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Univ. of Michigan
CMOS → MEMS 2

UCB Poly-SiGe Process

- 3 μm standard CMOS process, Al metallization
- p-type poly-Si$_{0.35}$Ge$_{0.65}$ structural; poly-Ge sacrificial
- MEMS-CMOS interconnect through p-type poly-Si strap
- Process:
  - CMOS passivated with LTO, 400°C
  - Vias to connection strap opened
  - Ground plane deposited, MEMS built.
  - RTA anneal to lower resistivity (550°C, 30s)

A. Franke PhD
General observations

- Each of the combination methods
  - Limited in versatility and dissemination
  - Processing "modules" would need a lot of investments for each new upgrade
- It is striking to observe the enormous investments in the IC industry for developing standardized and powerful CMOS processes with still finer line dimensions and higher speed

- Why not using an ordinary CMOS process: CMOS – MEMS?
  - One way of implementing CMOS – MEMS
    - ASIMPS run by CMP ("Circuits Multi-Projets")
    - ST Microelectronics, ST7RF BiCMOS, 0.25µm
    - Postprocessing at Carnegie Mellon University (CMU)
  - A CMOS – MEMS test circuit has been developed at the NANO group
    - Jan Erik Ramstad: CMOS – MEMS oscillator
    - Jostein Ekre: CMOS – MEMS inductors
Figure 1. ST7RF CMOS MEMS process flow. (a) Foundry CMOS before micromachining; (b) CHF$_3$/O$_2$ reactive-ion etch of dielectric stack down to the silicon substrate; (c) Deep reactive-ion etch of Si substrate (nominal 35 $\mu$m deep); and (d) Si undercut (nominal 15 $\mu$m undercut and 50 $\mu$m deep).
- Standard CMOS is used
- MEMS structures: **Multilayer stack** of metals and dielectrics
  - reduced Youngs modulus \( (E = \text{stiffness}) \)
  - not so good material as polySi/poydiamond used in specialized MEMS processes
- Metal layer used as mask
  - 5 metal layers
  - any one can be used as a mask defining the thickness of the mechanical structure
- MEMS devices released in a mask-less etch & release process
  - high aspect ratio RIE + isotropic etch of underlying substrate
  - done chip-wise on individual diced chips
  - no extra masks needed for MEMS \( \rightarrow \) MPW can be used
  - active CMOS circuit area must be completely covered by metal
- Specific MEMS design rules
  - determine released or anchored areas
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Master project (finished)

- Integrated MEMS/CMOS oscillator
  - based on a resonating cantilever beam

- Master student Jan Erik Ramstad (Bachelor HiVe)
- MEMS resonator with CMOS feedback amplifier
- To be used as a "resonant detector"
  - a mechanical resonating structure where physical measurement parameters modify the resonant frequency
  - e.g. sensing acceleration

- Investigate possibilities for monolithic integration
  - post CMOS micromachining
Cantilever beam

- Principle of operation
  - The beam is attracted by the electrostatic forces between the electrode and beam
  - A DC voltage over the gap amplifies the el-mech coupling
  - Contributions off the fundamental frequency can be omitted

Equivalent diagram of the cantilever beam

$k, m, b \rightarrow C, L, R$
Design example

- A CMOS – MEMS oscillator
- Blockdiagram
  - vibrating cantilever beam coupled in loop with a feedback Pierce CMOS amplifier
  - oscillation at a frequency given by the characteristic resonating mode of the cantilever beam modified by the input and output capacitances of the Pierce amplifier

[JER]
Vibrating beam used as a sensor

- External acceleration will bend the beam
  - the spring coefficient of the beam is slightly altered
  - the frequency is changed and can be observed
- Beam layout
  - laminated structure of 4 Al layers + SiO2
  - 4.8 µm thickness (W) x 2 µm width (H)
  - length = 100 (60) µm, gap = 1.2 µm
Oscillation criterion

- "Motional resistance" of the beam, $R_x$
  - A critical parameter
  - Dependent of the gap and overlap area for electrostatic actuation
  - A low $R_x$ is desirable
    - small gap! – dependent on processing resolution and polymer coating
    - large overlap area – thickness is limited by the laminated structure
    - $R_x \sim 700$ kohm

- "Barkhausen criterion"
  - The negative input resistance $Re(Z_c)$ must be at least 3x larger than $R_x$ for oscillation to start up (by thermal noise!)
  - The negative resistance is controlled by tuning the Pierce capacitors $C_1$, $C_2$, $g_m$ and feedback resistor
  - $Re(Z_c)$ will change during startup and will stabilize when $R_x$ and $Re(Z_c)$ become equal
Design parameters - layout

- **Layout**
  - The gap of the cantilever beam must have a DC voltage across
    - introduced by a resistor and coupling capacitance (one-port structure)
    - (a two-port structure: decreased resolution)
- The design has been modeled and simulated
  - 3 designs (frequencies 120, 150, 480 kHz)

<table>
<thead>
<tr>
<th>Design #1</th>
<th>Design parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonance frequency, $f_0$ [kHz]</td>
<td>121.67</td>
</tr>
<tr>
<td>Pull-in voltage, $V_{pl}$ [V]</td>
<td>15.78</td>
</tr>
<tr>
<td>Motional current, $i_o$ [nA]</td>
<td>2.65</td>
</tr>
<tr>
<td>Deflection, $z$ [µm]</td>
<td>165.1</td>
</tr>
<tr>
<td>Negative resistance $Re(Z_e)$ [MΩ]</td>
<td>25.2</td>
</tr>
<tr>
<td>Max. neg. res. $Re(Z_e(\text{max}))$ [MΩ]</td>
<td>64.7</td>
</tr>
<tr>
<td>Motional resistance, $R_z$ [kΩ]</td>
<td>203.6</td>
</tr>
<tr>
<td>Motional inductance, $L_z$ [H]</td>
<td>1066</td>
</tr>
<tr>
<td>Motional capacitance, $C_z$ [aF]</td>
<td>1607</td>
</tr>
<tr>
<td>Nominal Q-factor, $Q$</td>
<td>4000</td>
</tr>
</tbody>
</table>

**Dimensions**
- Height, $H$ [µm] | 2
- Width, $W$ [µm] | 4.8
- Length, $L$ [µm] | 100
- Electrode length, $W_e$ [µm] | 75
- Electrode gap, $g$ [µm] | 1.2
Test circuit

Sent to production in January 2007

1. System #1 - L=100u, W=4.8u, Wc=75u, H=2u, g=1.2u
2. System #2 - L=60u, W=4.8u, Wc=45u, H=1, g=1.2u
3. System #3 - L=100u, W=4.8u, Wc=80u, H=1u, g=1.2u (CC-beam)
4. System #4 - Identical to system #1, used as test structures
FROM MEMS DEVICES TO SMART INTEGRATED SYSTEMS
O. Sørhaugen and J. E. Ramstad
Dept. of Informatics, University of Oslo, P.O. Box 1088 Blindern, N-0316 Oslo, Norway
eddvar@ifi.uio.no  janera@student.maatet.uio.no

Key factors:
• Osmosis coupling of a MEMS recording cantilever beam and a CMOS pickup amplifier
• Actuation is governed by a frequency change of the recording cantilever beam
• Micro-integration of the system using post-CMOS packaging
• RPAW from "Circuits Multi-Projects"
• 0.25 um CMOS from ST Microelectronics
• post-processing at Carnegie Mellon University
• This approach is feasible for implementing future integrated systems.

Implementation using a CMOS process:

System block diagram:

- MEMS and CMOS integrated on one chip
- The Phono amplifier is followed by a racetrack modulator of a MEMS cantilever beam which is driven by a PFE

Cantilever beam:

- Beam length L=100 u, width W=184 u, height H=5 u
- The cantilever beam is deflected by applying a 50 Vpp d.c.

Layout:

- resulting layout for MEMS cantilever and accompanying CMOS circuits
- Metal layer 5 covers the complete area, except for the MEMS cantilever beam which is surrounded by a yellow rectangle
- Also not shown: metal layer 6 is etched through the cantilever beam is released as a free-standing structure

Pierce amplifier:

- Capacitors C1 and C2 and the transconductance from transistor M1 controls the negative resistance R0

Design results and parameters:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>Range</td>
<td>1.8 MHz</td>
</tr>
<tr>
<td>Bias current</td>
<td>-1.8 uA</td>
</tr>
<tr>
<td>Noise figure</td>
<td>20 nV/Hz</td>
</tr>
</tbody>
</table>
Master project (finished)

- RF transceiver for a Wireless Sensor Node
  - Medical application
  - Brain pressure sensor
  - Built-in intelligence
  - Robust
  - Low-power

- Master student Jostein Ekre
  - Design and demonstration of critical RF MEMS parts
  - Interfacing and implementation issues
MEMS inductors are vital for implementing WSNodes.

Planar coils made from multiple metal layers
The same test circuit did also contain MEMS inductors
Ex. from CMU: "C, L resonator tank"
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The future: "From devices → systems"

- Future smart systems would require **combination of technologies**
  - e.g. integrated CMOS – MEMS systems
  - Micro og nano sensors integrated with complex electronics will be used in distributed, ubiquitous systems, medical implants etc.

- The ASIMPS method could be one way for a group of applications
  - using "many", "non-optimal" MEMS devices
  - effective interfacing to electronics
  - → high performance systems
  - enhanced performance due to process upgrading
Activities

- SINTEF project
  - CMOS – MEMS at MiNaLAB
  - part of SIP
Activities

- **SINTEF project**
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- **New Master project:** *Combination of microelectronics (CMOS) og miniaturized mechanical components (RF MEMS) for reconfigurable “radio-on-a-chip front-end”*
  - **varactor (variable reactor)** is central for reconfigurability
    - VCO (voltage controlled oscillator)
    - designing for maximum tuning range and high performance

- **New Ph.D. project:** *Micromachined RF front-end modules integrated with standard CMOS microelectronics in smart wireless sensor networks*
  - RF MEMS resonating CMOS – MEMS structures
Personal research goals

1) Designing RF MEMS and investigating how to use high performance micromechanical replacement parts in RF systems instead of today's bulky and power consuming off-chip components.

2) Investigating effective methods for integration of the MEMS with microelectronic subsystems, preferably as a monolithic Si chip (SoC).

→ Critical technology and realistic implementations of Wireless Sensor Nodes.